



# STD70N03L STD70N03L-1

N-channel 30V - 0.0059Ω - 70A - DPAK / IPAK  
STripFET™ III Power MOSFET

## General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD70N03L	30V	<0.0073Ω	70A
STD70N03L-1	30V	<0.0073Ω	70A

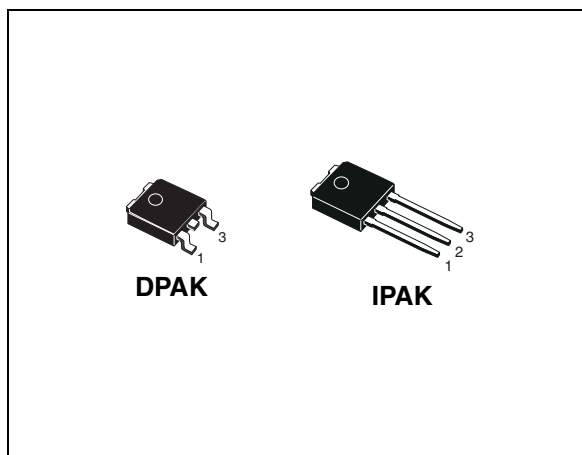
- R<sub>DS(ON)</sub> \* Qg industry's benchmark
- Conduction losses reduced
- Switching losses reduced
- Low threshold device

## Description

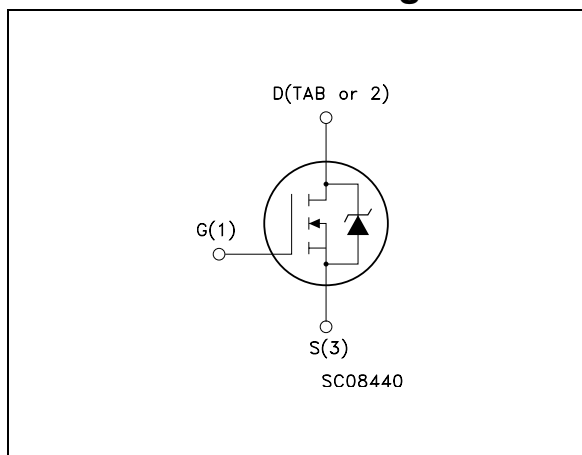
This product utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

## Applications

- Switching application



## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STD70N03L	D70N03L	DPAK	Tape & reel
STD70N03L-1	D70N03L-1	IPAK	Tube

# Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	70	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	50	A
$I_{DM}^{(1)}$	Drain current (pulsed)	280	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	70	W
	Derating factor	0.47	W/ $^\circ\text{C}$
$E_{AS}^{(2)}$	Single pulse avalanche energy	300	mJ
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2. Starting  $T_j = 25^\circ\text{C}$ ,  $I_D = 30\text{A}$ ,  $V_{DD} = 15\text{V}$

**Table 2. Thermal resistance**

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case Max	2.14	$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal resistance junction-amb Max	100	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	275	$^\circ\text{C}$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 20V,$ $V_{DS} = 20V, T_c = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 35A$		0.0059	0.0073	$\Omega$
		$V_{GS} = 5V, I_D = 35A$		0.007	0.013	$\Omega$
		$V_{GS} = 10V, I_D = 35A @ T_j = 125^{\circ}C$		0.0091	0.0113	$\Omega$
		$V_{GS} = 5V, I_D = 35A @ T_j = 125^{\circ}C$		0.0108	0.0201	$\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10V, I_D = 15A$		40		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1MHz, V_{GS} = 0$		2200 380 49		pF pF pF
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 15V, I_D = 70A$ $V_{GS} = 5V$ <i>(see Figure 7)</i>		15.7 8.3 3.4	21	nC nC nC
$Q_{gls}^{(2)}$	Third-quadrant gate charge	$V_{DS} < 0V, V_{GS} = 10V$		15		nC
$R_G$	Gate input resistance	$f = 1MHz$ Gate DC Bias = 0 Test signal level = 20mV open drain		1.5		$\Omega$

1. Pulsed: pulse duration = 300 $\mu s$ , duty cycle 1.5%

2. Gate charge for synchronous operation: see [Appendix A: Power losses estimation](#)

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15V, I_D=35A,$ $R_G=4.7\Omega, V_{GS}=5V$ <i>(see Figure 13)</i>		21		ns
$t_r$	Rise time			95		ns
$t_{d(off)}$	Turn-off delay time			19		ns
$t_f$	Fall time			15		ns

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				70	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				280	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=35A, V_{GS}=0$			1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 70A,$ $di/dt=100A/\mu s,$ $V_{DD}=20V, T_j=150^\circ C$ <i>(see Figure 18)</i>		32		ns
$Q_{rr}$	Reverse recovery charge			51		nC
$I_{RRM}$	Reverse recovery current			3.2		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

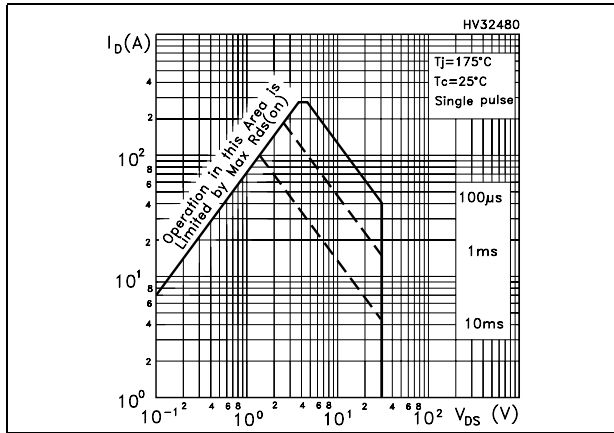


Figure 2. Thermal impedance

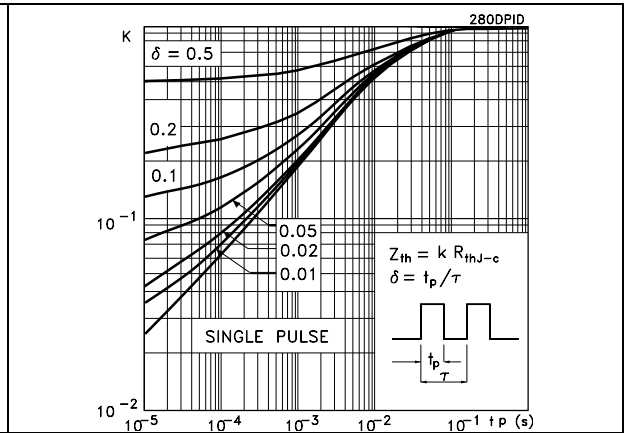


Figure 3. Output characteristics

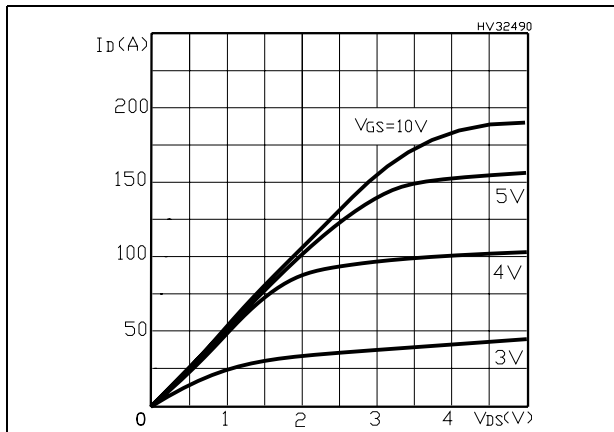


Figure 4. Transfer characteristics

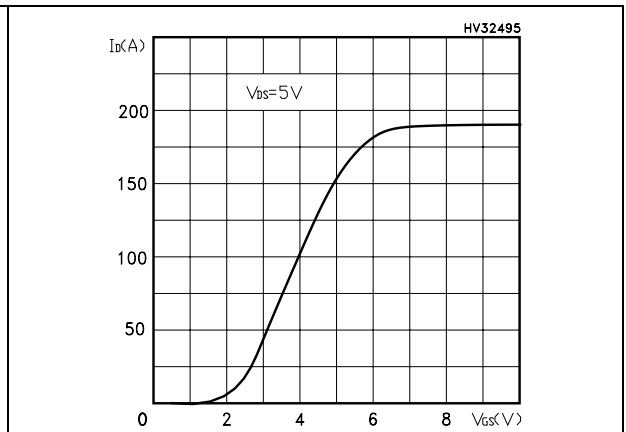


Figure 5. Transconductance

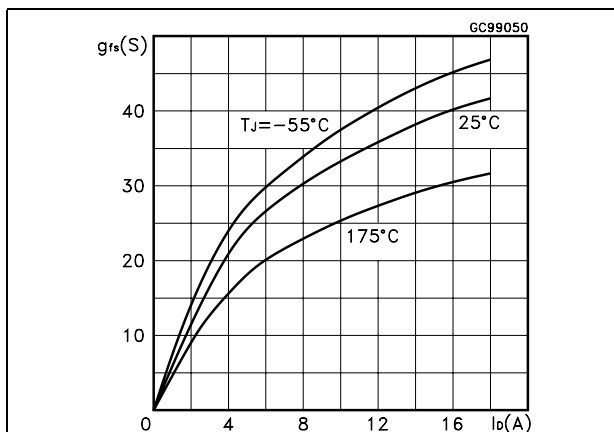


Figure 6. Static drain-source on resistance

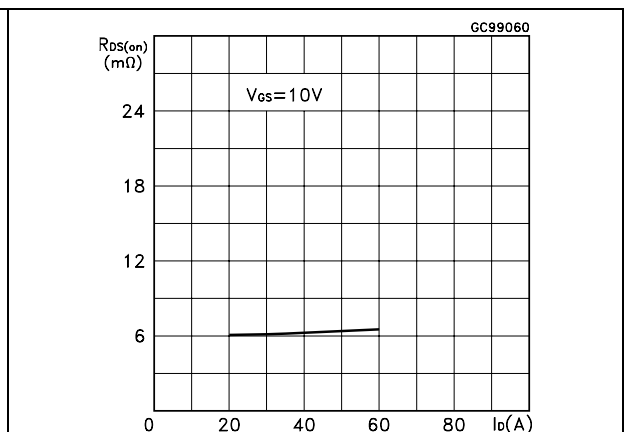


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

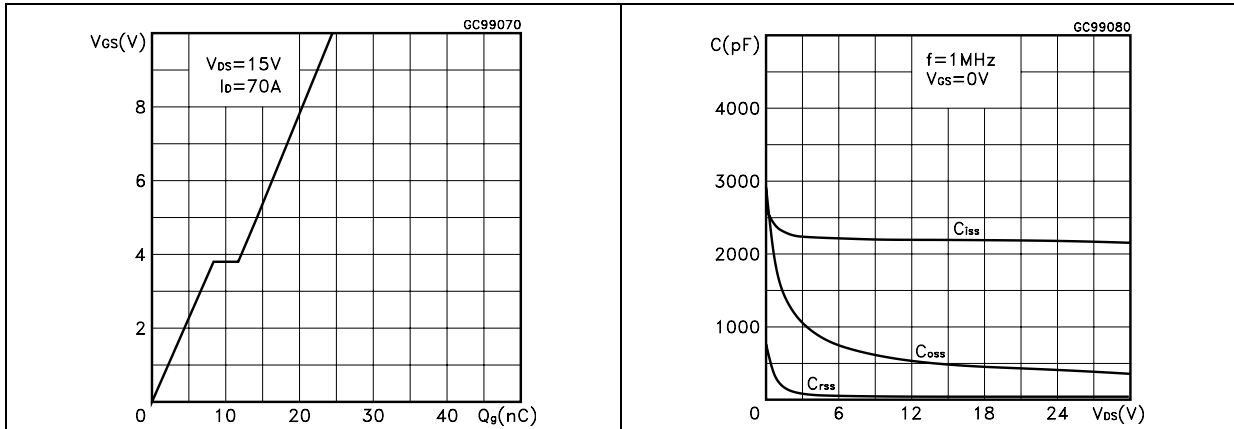


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

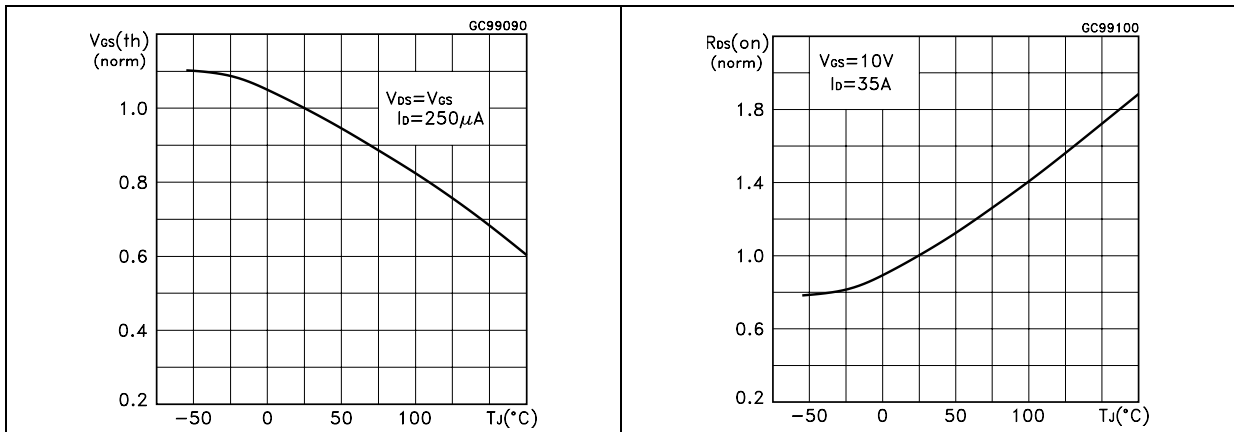
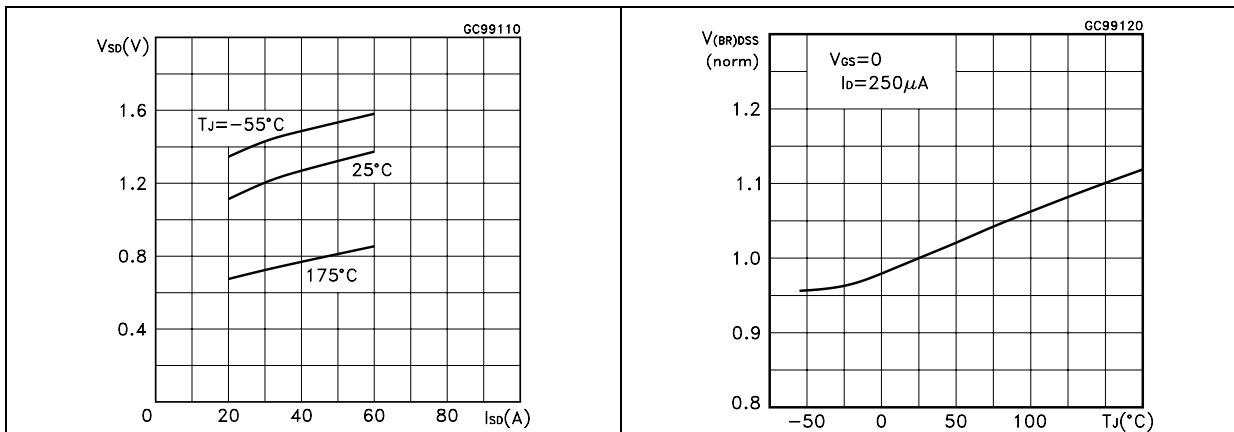


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized  $B_{V_{DS}}$  vs temperature



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

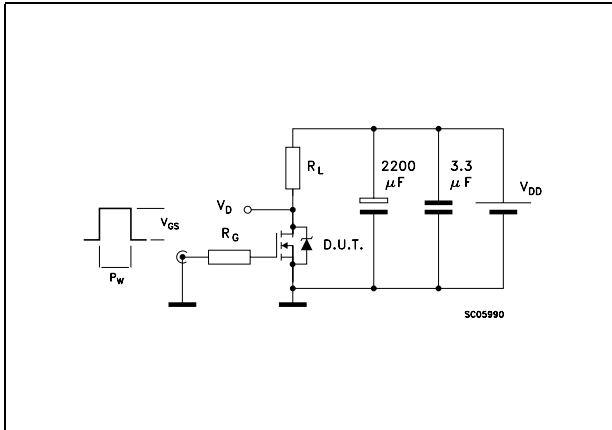


Figure 14. Gate charge test circuit

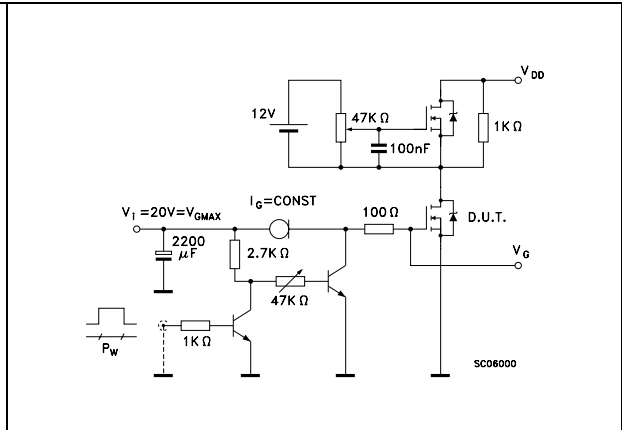


Figure 15. Test circuit for inductive load switching and diode recovery times

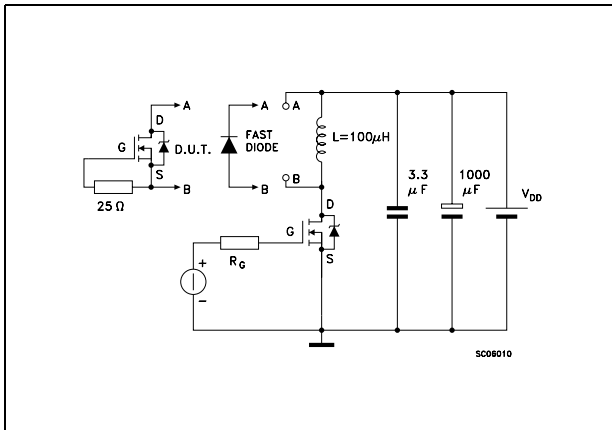


Figure 16. Unclamped inductive load test circuit

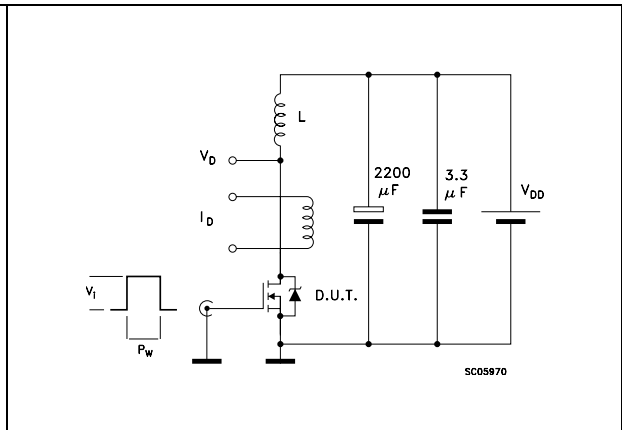


Figure 17. Unclamped inductive waveform

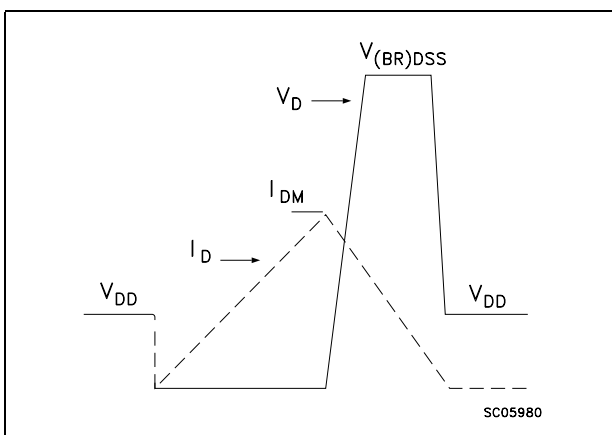
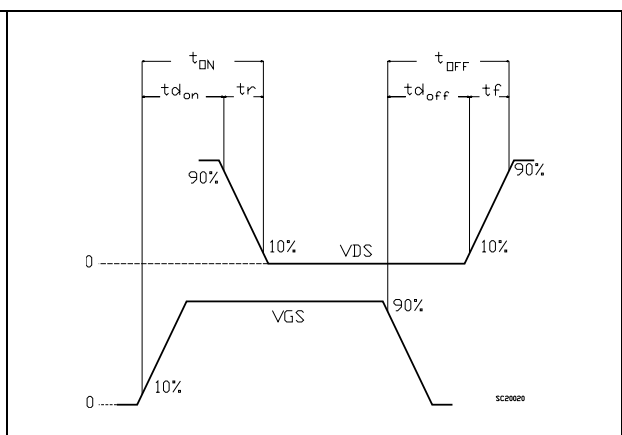


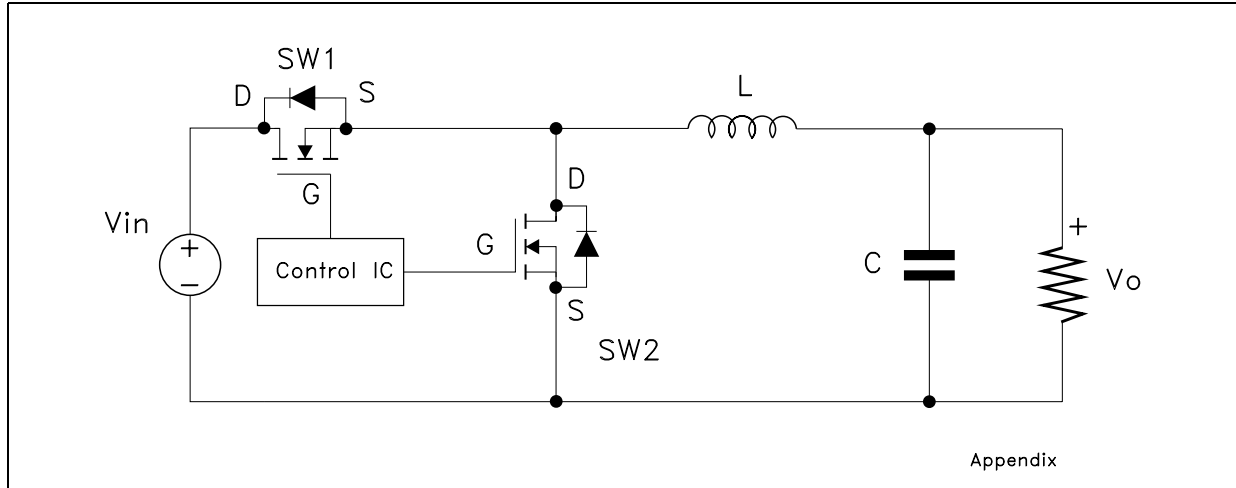
Figure 18. Switching time waveform





## Appendix A Power losses estimation

Figure 19. Buck converter



The power losses associated with the FETs in a synchronous buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (SW2) device requires:

- Very low  $R_{DS(on)}$  to reduce conduction losses
- Small  $Q_{gls}$  to reduce the gate charge losses
- Small  $C_{oss}$  to reduce losses due to output capacitance
- Small  $Q_{rr}$  to reduce losses on SW<sub>1</sub> during its turn-on
- The  $C_{gd}/C_{gs}$  ratio lower than  $V_{th}/V_{gg}$  ratio especially with low drain to source voltage to avoid the cross conduction phenomenon.

The high side (SW1) device requires:

- Small  $R_g$  and  $L_g$  to allow higher gate current peak and to limit the voltage feedback on the gate
- Small  $Q_g$  to have a faster commutation and to reduce gate charge losses
- Low  $R_{DS(on)}$  to reduce the conduction losses

		High side switch (SW1)	Low side switch (SW2)
$P_{\text{conduction}}$		$R_{\text{DS(on)}} \cdot I_L^2 \cdot \delta$	$R_{\text{DS(on)}} \cdot I_L^2 \cdot (1 - \delta)$
$P_{\text{switching}}$		$V_{\text{in}} \cdot (Q_{\text{gsth(SW1)}} + Q_{\text{gd(SW1)}}) \cdot f \cdot \frac{I_L}{I_g}$	Zero voltage switching
$P_{\text{diode}}$	Recovery	Not applicable	$V_{\text{in}} \cdot Q_{\text{rr(SW2)}} \cdot f$
	Conduction	Not applicable	$V_{\text{f(SW2)}} \cdot I_L \cdot t_{\text{deadtime}} \cdot f$
$P_{\text{gate(Qg)}}$		$Q_{\text{g(SW1)}} \cdot V_{\text{gg}} \cdot f$	$Q_{\text{gls(SW2)}} \cdot V_{\text{gg}} \cdot f$
$P_{\text{Qoss}}$		$\frac{V_{\text{in}} \cdot Q_{\text{oss(SW1)}} \cdot f}{2}$	$\frac{V_{\text{in}} \cdot Q_{\text{oss(SW2)}} \cdot f}{2}$

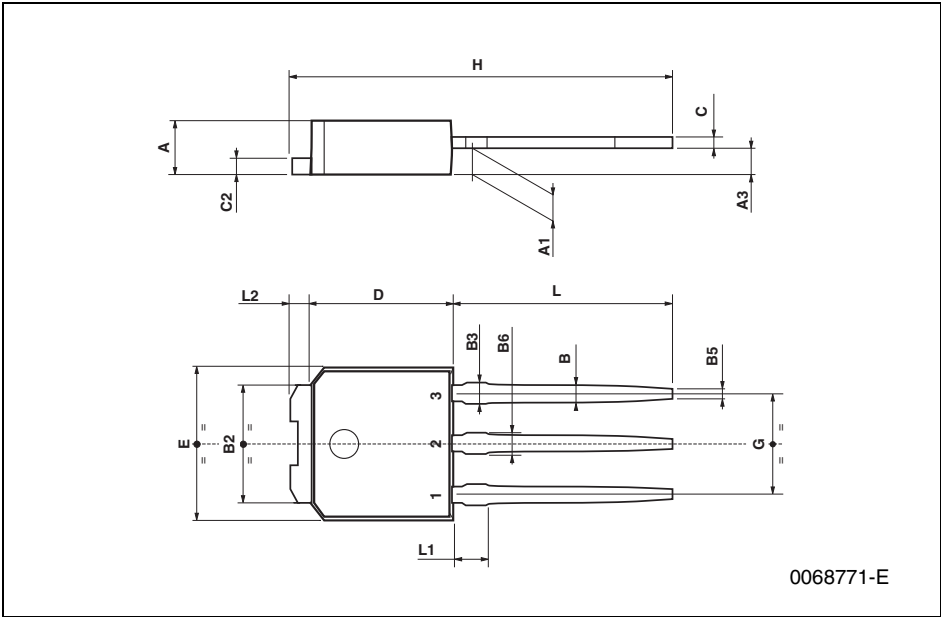
Parameter	Meaning
d	Duty-cycle
$Q_{\text{gsth}}$	Post threshold gate charge
$Q_{\text{gls}}$	Third quadrant gate charge
$P_{\text{conduction}}$	On state losses
$P_{\text{switching}}$	On-off transition losses
$P_{\text{diode}}$	Conduction and reverse recovery diode losses
$P_{\text{gate}}$	Gate driver losses
$P_{\text{Qoss}}$	Output capacitance losses

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

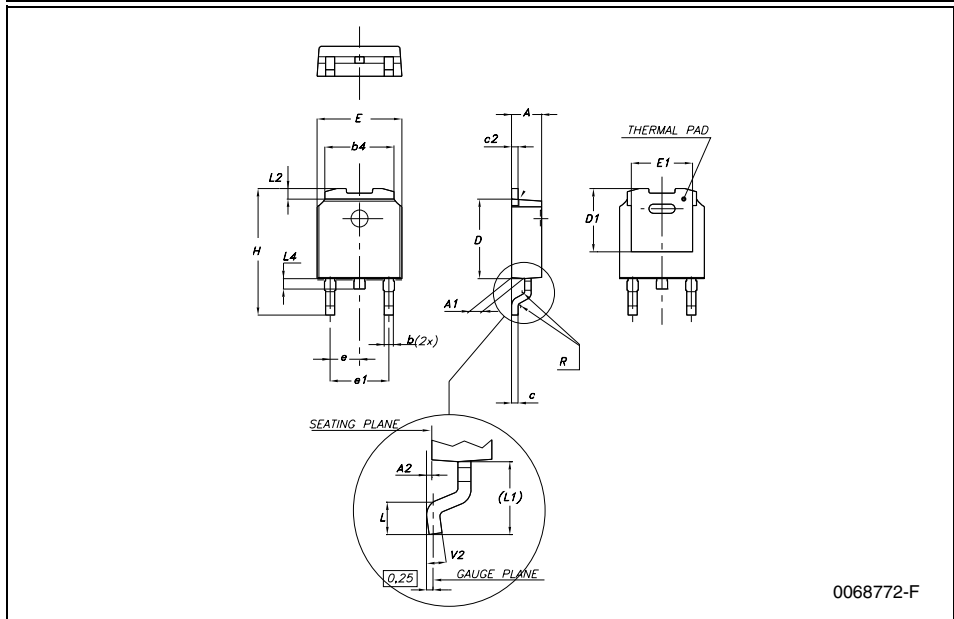
**TO-251 (IPAK) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



**DPAK MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



0068772-F

# 5 Packaging mechanical data

## DPAK FOOTPRINT



## TAPE AND REEL SHIPMENT

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

## 6 Revision history

Table 7. Revision history

Date	Revision	Changes
29-Jun-2006	1	First Release

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